

APR 20 2005

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RE: Y. Tanabe, et al., US Appl'n No. 10/774,589

Att'y Docket No. 501.37465CC9

Examiner David Vu, AU 2818, USPTO Conf. No. 1087

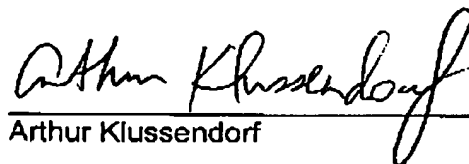
**SUBMISSION OF: Comments On Statement Of Reasons For Allowance,  
Information Disclosure Statement Under 37 CFR 1.97 And 1.98 and Credit Card  
Payment Form**

Sir:

Applicant hereby submits the attached COMMENTS ON STATEMENT OF  
REASONS FOR ALLOWANCE (2 pages), INFORMATION DISCLOSURE  
STATEMENT UNDER 37 CFR 1.97 AND 1.98 and documents submitted therewith  
(46 pages) AND PTO-2038 (1 page) for entry in the above-noted application.

**CERTIFICATE OF TRANSMISSION:**

I hereby certify that the attached COMMENTS ON STATEMENT OF  
REASONS FOR ALLOWANCE (2 pages), INFORMATION DISCLOSURE  
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(46 pages) AND PTO-2038 (1 page) are being **FORMALLY TRANSMITTED** via the  
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501.37465CC9

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APR 20 2005

Applicants: Y. TANABE, et al.

Serial No.: 10/774,589

Filed: February 10, 2004

Title: METHOD FOR FABRICATING SEMICONDUCTOR INTEGRATED  
CIRCUIT DEVICE

Group: 2818

Examiner: David Vu

Confirmation No.: 1087

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE**Mail Stop: ISSUE FEE**

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia 22313-1450

April 20, 2005

SIR:

The undersigned notes the Examiner's Statement of Reasons For Allowance, in Item 1 on page 2 of the Notice of Allowability enclosed with the Notice of Allowance and Fee(s) Due mailed February 9, 2005, in the above-identified application. This Statement sets forth that none of the references of record teaches or suggests a method for fabricating a semiconductor integrated circuit device, comprising specified steps.

More precisely, and in connection with the steps specified by the Examiner, and rather than the specified steps, it is respectfully submitted that the references do not disclose, nor would have suggested, such method comprising the steps of (a) forming an isolation groove between a plurality of active regions in a first major surface of a wafer; (b) forming an insulating region in the isolation groove by depositing an insulating layer; (c) synthesizing water vapor from oxygen and hydrogen gases by use of a catalyst; (d) keeping the synthesized water vapor in a gaseous state and feeding it into a processing chamber to form a wet oxidative atmosphere; and, (e) after forming the insulating region in the isolation groove as specified previously, performing thermal oxidation treatment to a silicon circuit portion over one of the active regions to form an insulating film under the

Docket No. 501.37465CC9  
Serial No. 10/774,589  
April 20, 2005

wet oxidative atmosphere in the processing chamber, as well as other features of the present invention as set forth in the allowed claims.

The undersigned also notes the concurrently filed Information Disclosure Statement Under 37 CFR 1.97 and 1.98, for submitted documents cited in a Supplementary Partial European Search Report in connection with an European Patent Application corresponding to the above-identified application, these documents to be considered by the Examiner prior to issuance of a U. S. Patent based upon the above-identified application. As set forth in the concurrently filed Information Disclosure Statement, present filing of this Information Disclosure Statement satisfies all applicable requirements of 37 CFR 1.97 and 1.98, with respect to the submitted documents, for the above-identified application. Consideration of the submitted documents; and, subsequent thereto, issuance of a U. S. Patent based upon the above-identified application in due course, are respectfully requested.

Entry of the present comments of record in the above-identified application is respectfully requested.

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 501.37465CC9).

Respectfully submitted,  
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